



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Takahisa YAMAHA

Date: October 16, 2001

Serial No.: 09/518,709

Group Art Unit: 2812

Filed: March 3, 2000

Examiner: Jerome Jackson, Jr.

For: MANUFACTURE METHOD FOR SEMICONDUCTOR WITH SMALL VARIATION IN
MOS THRESHOLD VOLTAGE

Asst. Commissioner for Patents
Washington, D.C. 20231

RESPONSE TO ELECTION/RESTRICTION REQUIREMENT

Sir:

REMARKS

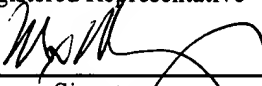
Applicant is responding herein to the Election/Restriction Office Action dated August 28, 2001, interposing a restriction requirement between two groups of claims.

Applicant is hereby electing to prosecute the claims of Group II, Claims 14-21, drawn to a semiconductor, classified in class 257, subclass 288.

It is noted that the entry of the restriction requirement reflects and makes of record, the Patent Office position that the two groups of claims are directed to different inventions.

Early and favorable consideration of the present application is earnestly solicited.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Asst. Commissioner for Patents, Washington, D.C. 20231, on October 16, 2001

Max MoskowitzName of applicant, assignee or
Registered Representative
Signature
October 16, 2001
Date of Signature

Respectfully submitted,


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